Amendments to the Specification:

Please replace Paragraph [0034] as filed with the following amended paragraph:

[0034] To reduce the defects of power bounce and cross talk found in the prior art, there are two main differences between the present invention and the prior art. First, the network interface circuit 50 in the present invention could reset different PHY circuits at different times, so each PHY circuit starts to operate at a different time. There are two ways to realize the interlacing of the reset times of different PHY circuits. As illustrated in Fig.4, in the present invention, different reset circuits 66A and 66B are set as the control circuits of the PHY circuits 54A and 54B respectively. Reset signals 68A and 68B are utilized to trigger reset ends RS3 and RS4 for resetting the PHY circuits. Assuming the PHY circuits in Fig.4 get reset when receiving a digital 1 as a reset signal, the reset circuits 66A and 66B generate corresponding reset signals 68A and 68B with ~~registers~~ resistors Ra and Rb and capacitors Ca and Cb under the DC voltage biasing source respectively, as illustrated in Fig.4. The DC voltage source V can be the DC biasing voltage source of the network interface circuit 50. When the network interface circuit 50 starts to function, the DC voltage source V charges the capacitors Ca and Cb through the ~~registers~~ resistors Ra and Rb respectively. Taking the reset circuit 66A for example, the potential of the capacitor Ca at node N0 is charged from the low level to the high level, and the reset signal 68A then changes from a digital 0 to digital 1. It is known that, as the product of the capacitor and the resistor changes in a charging circuit, the time constant of the circuit changes. In other words, as long as the products of the capacitor and the resistor in the reset circuits 66A and 66B, Ra*Ca and Rb*Cb, are different, the reset signals 68A and 68B change from digital 0s to digital 1s at different times, and hence the PHY

circuit 54A and 54B are reset at different times. In addition, the MAC circuit 52 controls the PHY circuits to reset by sending commands to the control ports CL3 and CL4. As long as the MAC circuit 52 could send the reset commands at different times, the PHY circuit 54A and 54B can reset at different times.